CLAIMS

WHAT IS CLAIMED IS:

1. A method for hierarchical Z buffering and stenciling comprising:

comparing a tile Z value range with a hierarchical Z value range and a stencil code;

updating the hierarchical Z value range and the stencil code in response thereto; and

determining whether to render a plurality of pixels within the tile based on the comparison of the tile with the hierarchical Z value range and the stencil code.

2. The method of claim 1 wherein the step of determining whether to render a plurality of pixels further comprises:

determining at least one of the following: (1) if a stencil test fails, (2) if the stencil test passes and a hierarchical Z value test fails and (3) if the stencil test passes and the hierarchical Z value test passes on at least one pixel in the tile.

3. The method of claim 2 further comprising:

rendering the pixels of the tile when the stencil test passes and the hierarchical Z value test passes on at least one pixel in the tile.

4. The method of claim 2 further comprising:

killing the tile when at least one of the following occurs: the stencil test fails or the stencil test passes and the hierarchical Z value test fails.

5. The method of claim 1 wherein the tile Z value range contains a tile MinZ and a tile MaxZ and the hierarchical Z value range contains a hierarchical cache MinZ and a hierarchical cache MaxZ.

6. The method of claim 5 wherein the stencil code is a three bit data value representing a range of stencil values in the tile relative to a background value.

7. The method of claim 1 wherein the step of determining whether to render a plurality of pixels further comprises:

determining if a per-pixel depth operation needs to be performed; and

determining if stencil operations need to be performed.

8. A method for hierarchical Z buffering and stenciling comprising:

(a) receiving a tile having a plurality of pixels;

(b) determining if the tile is visible relative to a stencil; and

(c) determining if the tile is visible in a hierarchical Z plane.

9. The method of claim 8 further comprising:

(d) generating an indicator to indicate whether to render the plurality of pixels within the tile.

10. The method of claim 9 wherein the decision whether to render the plurality of pixels within the tile includes:

determining if a per-pixel depth operation needs to be performed; and

determining if stencil operations need to be performed.

11. The method of claim 8 wherein step (b) further comprises:

(b1) generating a stencil code; and

(b2) comparing the stencil code to a stencil value and a stencil mask.

12. The method of claim 11 wherein the stencil code is a multiple-bit indicator which specifies the relation of a plurality of stencil values in the tile relative to a background value.

13. The method of claim 11 wherein step (c) further comprises:

(c1) receiving a MinZ and a MaxZ for the tile;

(c2) comparing the MinZ and the MaxZ to a hierarchical Z range; and

(c3) wherein at least one of the plurality of pixels is visible in the z-plane, indicating the tile is visible in the hierarchical Z plane.

14. The method of claim 12 further comprising:

generating an indicator, wherein the indicator indicates at least one of the following: a positive indication when it is determined that the tile is visible relative to the stencil and it is determined that the tile is visible in the hierarchical Z plane and a negative indication when it is determined that the tile is not visible relative to the stencil or it is determined that the tile is not visible in the hierarchical Z plane.

15. The method of claim 14 wherein the pixels of the tile are rendered if the indicator indicates a positive indication and wherein the tile is killed if the indicator indicates a negative indication.

16. The method of claim 11 further comprising:

(e) updating a hierarchical Z value range and a stencil code in response thereto.

17. An apparatus for hierarchical Z buffering and stenciling comprising:

a comparator;

a hierarchical Z buffer and stencil cache operably coupled to the comparator; and

a hierarchical Z buffer and stencil cache updater operably coupled to the comparator wherein the hierarchical Z buffer and stencil cache provides a cache MinZ, cache MaxZ, and stencil code to the comparator.

18. The apparatus of claim 17 further comprising:

a tile comprising a plurality of pixels wherein the tile has a tile MinZ and a tile MaxZ.

19. The apparatus of claim 18 wherein the comparator receives the tile MinZ and the tile MaxZ and compares the tile MinZ and the tile MaxZ to the cache MinZ, the cache MaxZ, and the stencil code to determine if a per-pixel depth operation needs to be performed and to determining if stencil operations need to be performed..

20. The apparatus of claim 19 wherein the comparator generates an indicator that indicates the visibility of the plurality of pixels of the tile relative a stencil mask and a hierarchical Z plane.

21. The apparatus of claim 20 further comprising:

a kill module operably coupled to the hierarchical Z buffer and stencil cache updater wherein the hierarchical Z buffer and stencil cache updater receives the indicator from the comparator and the hierarchical Z buffer and stencil cache updater provides a kill signal to the kill module based on the indicator.

22. The apparatus of claim 21 wherein the hierarchical Z buffer and stencil cache updater updates the hierarchical Z buffer and stencil cache in response to the indicator.

22. A graphics processing engine comprising:

a tile comprising a plurality of pixels wherein the tile has a tile MinZ and a tile MaxZ;

a comparator;

a hierarchical Z buffer and stencil cache operably coupled to the comparator ; and

a hierarchical Z buffer and stencil cache updater operably coupled to the comparator wherein the hierarchical Z buffer and stencil cache provides a cache MinZ, cache MaxZ, and stencil code to the comparator, wherein the comparator receives the tile MinZ and the tile MaxZ and compares the tile MinZ and the tile MaxZ to the cache MinZ, the cache MaxZ, and the stencil code..

23. The apparatus of claim 22 wherein the comparator generates an indicator that indicates the visibility of the plurality of pixels of the tile relative a stencil mask and a hierarchical Z plane.

24. The apparatus of claim 23 further comprising:

a kill module operably coupled to the hierarchical Z buffer and stencil cache updater wherein the hierarchical Z buffer and stencil cache updater receives the indicator from the comparator and the hierarchical Z buffer and stencil cache updater provides a kill signal to the kill module based on the indicator and wherein the hierarchical Z buffer and stencil cache updater updates the hierarchical Z buffer and stencil cache in response to the indicator.